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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al.

Art Unit : 2123

Serial No. : 09/994,574

Examiner : Unknown

Filed : November 26, 2001

Title : UNIFIED DESIGN PARAMETER DEPENDENCY MANAGEMENT METHOD
AND APPARATUS

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT

Copies of the references listed on the attached form PTO-1449 are enclosed.

This statement is being filed before the receipt of a first Office action on the merits.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: _____

9/12/2003

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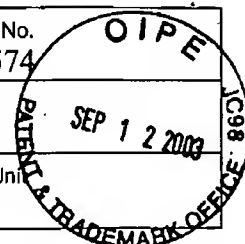
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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-602001	Application No. 09/994,574
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al.	
		Filing Date November 6, 2001	Group Art Unit

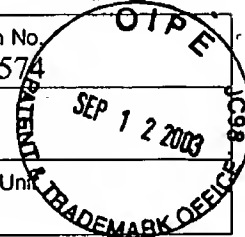


U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date if Appropriate
	AA	5,598,347	01/28/1997	Iwasaki			
	AB	RE 38,059	04/01/2003	Yano et al.			
	AC	6,574,787	06/03/2003	Anderson			
	AD	6,539,536	03/25/2003	Singh et al.			
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	AZ	4,703,435	10/27/1987	Darringer et al.			
	AAA						

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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		Filing Date November 6, 2001	Group Art Unit



Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	ABB	JP 2001068994	03/16/2001	Japan			Abstract only	
	ACC	EP 720233	07/03/1996	European Patent			X	
	ADD	JP 07049890	02/21/1995	Japan			Abstract only	
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Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AGG	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345 (7pages)
	AHH	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, 17 September 2000, pp. 487-493.
	AII	
	AJJ	

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